IN THE CLAIMS

What is claimed is:

1. An apparatus comprising:

dependency matching logic to receive a first dependency coordinate and a second dependency coordinate corresponding to a dependency relationship, the dependency matching logic, upon receiving the first and second dependency coordinates, to identify whether the first dependency precludes scheduling; and

dependency checking logic to produce a ready signal if the dependency matching logic has not identified that scheduling is precluded.

2. The apparatus of Claim 1 wherein the first dependency coordinate corresponds to a first buffer.

3. The apparatus of Claim 2 wherein the second dependency coordinate corresponds to first location within the first buffer.

4. The apparatus of Claim 2 wherein the first dependency coordinate corresponds to a buffer in an arrangement selected from the group of a hierarchical buffer arrangement, a functional buffer arrangement, and a symmetric buffer arrangement.

5. The apparatus of Claim 1 further comprising:

a scheduling information interface to transmit, to the dependency matching logic, a

dispatch signal pertaining to an instruction being dispatched, the dependency matching logic, upon receiving the dispatch signal to identify whether the first dependency precludes scheduling by matching the dispatch signal to the first and second dependency coordinates.

6. The apparatus of Claim 5 further comprising:

a write-enable input to transmit, to the dependency matching logic, a write-enable signal to enable the dependency matching logic to store the second dependency coordinate.

7. The apparatus of Claim 6 wherein the dependency matching logic, upon receiving the dispatch signal is to identify whether the first dependency precludes scheduling by clearing the second dependency coordinate.

8. The apparatus of Claim 7 wherein the dependency matching logic, upon receiving the dispatch signal is enabled to clear the second dependency coordinate while receiving the write-enable signal.

9. A method for scheduling an instruction for execution comprising:

generating a first dependency coordinate to indicate that a second instruction is dependent on a first instruction;

generating a second dependency coordinate to indicate that the second instruction is

dependent on the first instruction;

dispatching the first instruction for execution;

using the first dependency coordinate to access the second dependency coordinate in response to the first instruction being dispatched; and

dispatching the second instruction after accessing the second dependency coordinate.

10. The method of Claim 9 further comprising:

storing the first instruction in a first location corresponding to second dependency coordinate within a first buffer.

11. The method of Claim 10 wherein the first dependency coordinate indicates that the first instruction is stored in the first buffer.

12. An article of manufacture comprising

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the method of Claim 11.

13. A method for scheduling an instruction for execution comprising:

storing a first instruction in a first location within a first buffer;

storing a second instruction, dependent on the first instruction, in a second location within a second buffer;

generating a first dependency coordinate for the second instruction to indicate that the second instruction is dependent on an instruction stored in the first buffer; and

generating a second dependency coordinate for the second instruction to indicate that the second instruction is dependent on an instruction stored in the first location.

14. The method of Claim 13 further comprising:

dispatching the first instruction for execution;

matching the first dependency coordinate to a dispatch from the first buffer in response to the first instruction being dispatched;

matching the second dependency coordinate to a dispatch from the first location in response to the first instruction being dispatched; and

dispatching the second instruction after matching the first dependency coordinate and the second dependency coordinate.

15. A dependency matching logic comprising:

a first storage location to store a first dependency coordinate referencing one of a plurality of operation buffers;

a second storage location to store a second dependency coordinate referencing a location of a plurality of addressable locations in an operation buffer;

an interface to receive an indication of a first scheduled operation, the dependency matching logic, upon receiving the indication of the first scheduled operation, to identify whether the first scheduled operation corresponds to the location referenced by the second dependency coordinate in the buffer referenced by the first dependency coordinate.

16. The apparatus of Claim 15 further comprising:

a write-enable input to transmit, to the dependency matching logic, a write-enable signal to enable the dependency matching logic to store the second dependency coordinate.

17. The apparatus of Claim 16 wherein the dependency matching logic, is to clear the second dependency coordinate responsive to identifying that the first scheduled operation corresponds to the location referenced by the second dependency coordinate in the buffer referenced by the first dependency coordinate.

18. The apparatus of Claim 17 wherein the dependency matching logic, responsive to identifying that the first scheduled operation corresponds to the location referenced by the second dependency coordinate in the buffer referenced by the first dependency coordinate is enabled to clear the second dependency coordinate concurrent with the receiving of the write-enable signal.

19. A dependency matching logic comprising:

means for storing a first dependency coordinate referencing one of a plurality of operation buffers;

means for storing a second dependency coordinate referencing a location of a plurality of addressable locations in an operation buffer;

means for receiving an indication of a first scheduled operation; and

means for identifying whether the first scheduled operation corresponds to the

location referenced by the second dependency coordinate in the buffer referenced by the first dependency coordinate.

20. The apparatus of Claim 19 further comprising:

means for clearing the second dependency coordinate concurrent with the cycle in which it is received for storing.

21. An article of manufacture comprising:

a machine-accessible medium including data that, when accessed by a machine, cause the machine to:

generate a first dependency coordinate for a first instruction to indicate that the first instruction is dependent on an instruction stored in a first buffer;

generate a second dependency coordinate for the first instruction to indicate that the first instruction is dependent on an instruction stored in a first location in a buffer;

match the first dependency coordinate to a dispatching of a second instruction from the first buffer;

match the second dependency coordinate to a dispatching of the second instruction from the first location in the first buffer; and

dispatch the second instruction after matching the first dependency coordinate and the second dependency coordinate.

22. A computing system comprising:

dependency coordinate logic to store a first dependency coordinate referencing one of a plurality of operation buffers and a second dependency coordinate referencing a location of a plurality of addressable locations in an operation buffer;

dispatch logic coupled to the dependency coordinate logic to send an indication of a first scheduled operation;

dependency match logic to identify whether the first scheduled operation corresponds to the location referenced by the second dependency coordinate in the buffer referenced by the first dependency coordinate.

23. The computing system of Claim 22 further comprising:

fetch logic to receive a first instruction from a first memory; and

decode logic coupled with the fetch logic to translate the first instruction into at least one operation to be stored in one or more of the plurality of addressable locations in the operation buffer.

24. The computing system of Claim 22 wherein the decode logic comprises an integrated circuit.

25. The computing system of Claim 22 wherein the decode logic comprises a combination of an integrated circuit and emulation data.

26. The computing system of Claim 22 wherein the first instruction comprises an emulation instruction.

27. The computing system of Claim 22 wherein the first instruction comprises a macro-instruction.

28. The computing system of Claim 26 wherein the at least one operation comprises a micro-operation.

29. The computing system of Claim 26 wherein the at least one operation comprises an emulation instruction.